10.3 A 60GHz Low-Power Six-Port Transceiver for Gigabit Software-Defined Transceiver Applications

Chi-Hsueh Wang[1], Hong-Yeh Chang[2], Pei-Si Wu[1], Kun-You Lin[1], Tian-Wei Huang[1], Huei Wang[1], Chun Hsiung Chen[1]

[1]National Taiwan University, Taipei, Taiwan
[2]National Central University, Chungli, Taiwan

The unlicensed band around 60GHz provides the opportunity for high-data-rate wireless communications with reduced energy per bit. With the recent advances in semiconductor processing technology and the development of reconfigurable devices, the realization of high-bit-rate software-defined transceivers (SDTs) on a single chip has become practical. An SDT can change operating characteristics or parameters such as the operating frequency range, modulation scheme, bandwidth, and network protocols by programming [1]. Therefore, it can be reconfigured to solve interoperability problems between the many different existing communication standards, to implement new standards, and to minimize the amount of hardware necessary to perform required communications across these different standards. Six-port technique has been under development for many years. Recently, there has been reports that predicet the six-port receiver would replace the existing mixer-based architectures for SDR applications [1,2].

In this paper, a single-chip six-port transceiver platform for SDT application is presented. It achieves low cost, low complexity, low dc power, broad bandwidth, and reconfigurable architecture in a 0.13µm bulk CMOS technology with f_{max} and f_t of 108 and 91GHz, respectively. The block and schematic diagrams of this MMIC transceiver are shown in Figs 10.3.1 and 10.3.2, respectively. The transmitter is implemented using a reflection-type I/Q modulator which utilizes a 90° coupler to generate the quadrature-phase signals for the I/Q paths and an in-phase combiner to combine the I/Q modulated signals. The I/Q modulator also shows good sideband suppression with high local-oscillator suppression [3]. Low LO power is a very important feature in this six-port transceiver since the high signal power is difficult to obtain using CMOS at mm-wave frequencies. The six-port transceiver requires LO power level similar to the receiver input power which is much lower than that of other mixer-based approaches. The BA and LNA are implemented using six-stage cascode devices with matching networks implemented using thin film microstrip lines (TFMS) to achieve high-gain and low-noise performance with low DC power. The circuit topology similar to that reported in [4].

Both the BA and LNA have a similar gain of 20dB and noise figure of 8dB from 60 to 64GHz. The measured output 1dB compression of the BA is –2dBm including the loss of switch. The DC power consumption is 36.9mW for the BA and 31mW for the LNA. The VCO is measured via an extra test pad and has the measured frequency tuning range from 61.5 to 62.3GHz with output power of –12.1dBm at 62GHz and phase noise of –92.2dBc/Hz at 1MHz offset. The total DC power of the VCO is 30mW.

Figure 10.3.3 shows the measured conversion gain of the I/Q modulator including the BA versus LO frequency through the external LO port. From 60 to 64GHz, the measured image suppression is below 30dBc and the measured LO suppression is less than 20dBc. The second-order intermodulation components are less than 30dBc referenced to the desired output power and the third-order intermodulation components are less than 40dBc. The I/Q modulator is evaluated with a 5Mb/s 16QAM modulated signal with the channel power higher than –18dBm at 62GHz. The measured EVM of the 16QAM modulated signal is within 4.2%.

Figure 10.3.4 shows the measured output voltage of the power detector versus the receiver input power including the switch loss and gain of the LNA. The sensitivity is higher than 10000mV/mW when the input power is lower than –22dBm. For the six-port receiver, the phase and the ratio of amplitude between the LO signal and RF signal can be calculated from the power output at the other four ports. For the demodulation quality test, a 40Mb/s BPSK modulated signal is fed and its demodulated output signal is tested directly through vector signal analysis without calibration. The measured EVM of the BPSK signal is lower than 4% with an input power of –30dBm. A real-time six-port calibration method [2] is also adopted and the demodulation results for QPSK and 16QAM modulated signals are analyzed using ADS software. Figure 10.3.5 shows the output waveforms for QPSK and 16QAM demodulated signals after calibration. For high-data-rate applications, the transceiver is evaluated using signals of 4Gb/s data rate with BPSK modulation. Figure 10.3.6 shows the demodulation signal waveform with and without the calibration procedure.

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[2] X. Xu, R.G. Bosisio, and K. Wu "Analysis and Implementation of Six-Port Software-Defined Radio Receiver Platform," *IEEE Trans. MTT,* vol. 54, pp. 2937-2943, July, 2006.
[3] H.-Y. Chang, P.-S. Wu, T.-W. Huang, et al., "Design and Analysis of CMOS Broad-Band Compact High-Linearity Modulators for Gigabit Microwave/Millimeter-Wave Applications," *IEEE Trans. MTT,* vol. 54, pp. 20-30, Jan., 2006.
[4] C.-M. Lo, C.-S. Lin, and H. Wang, "A Miniature V-band 3-Stage Cascode LNA in 0.13µm CMOS," *ISSCC Dig. Tech. Papers*, pp. 402-403, Feb., 2006.

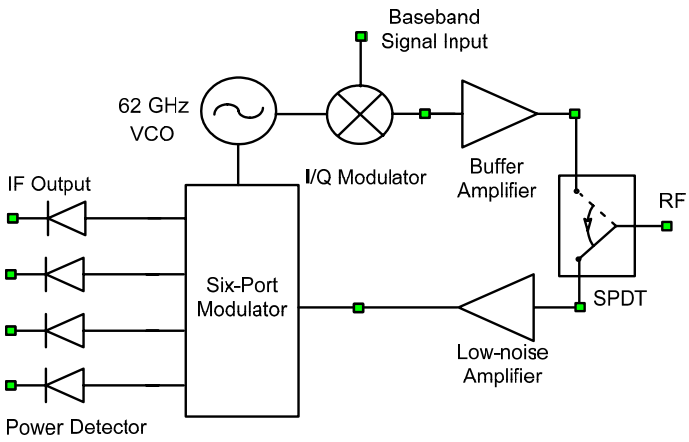

Figure 10.3.1: Block diagram of the 60GHz six-port transceiver.

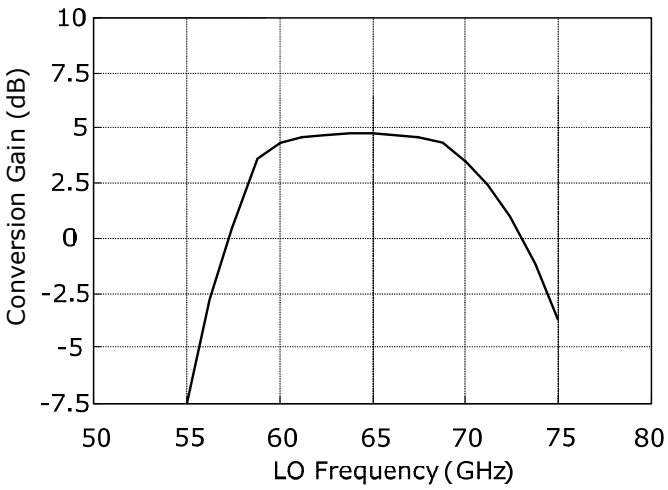

Figure 10.3.3: Transmitter conversion gain versus input LO frequency.

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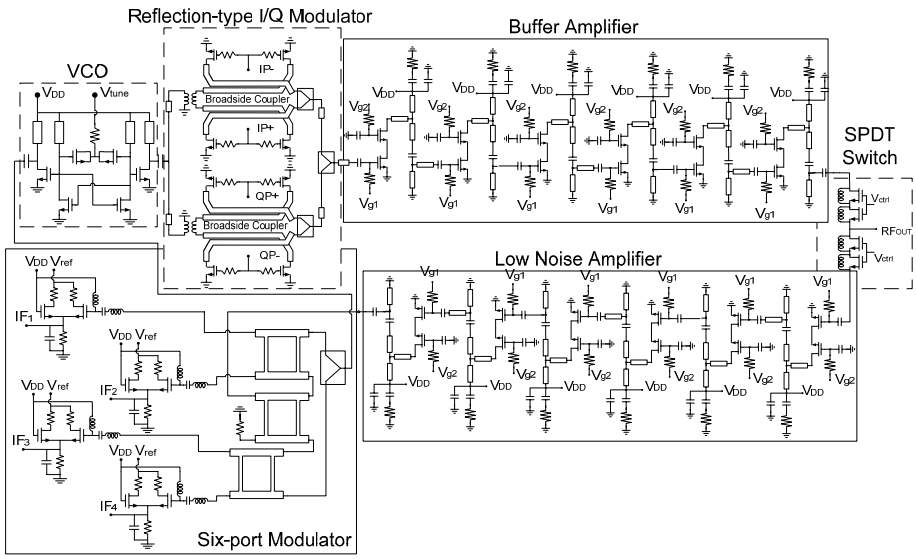

Figure 10.3.2: Schematic diagram of the 60GHz six-port transceiver.

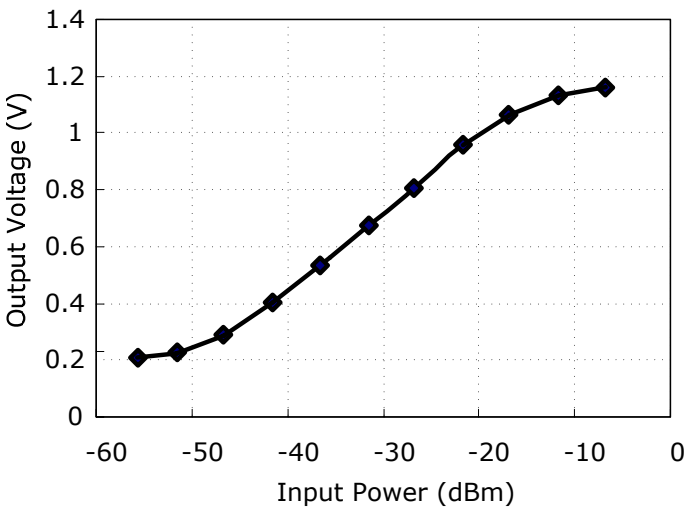

Figure 10.3.4: Measured output voltage versus receiver input power.

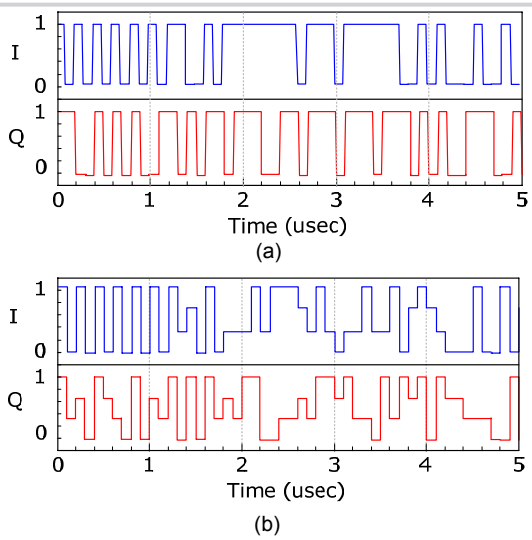

Figure 10.3.5: Measured demodulation signal waveforms after the calibration procedure: (a) QPSK and (b) 16QAM.

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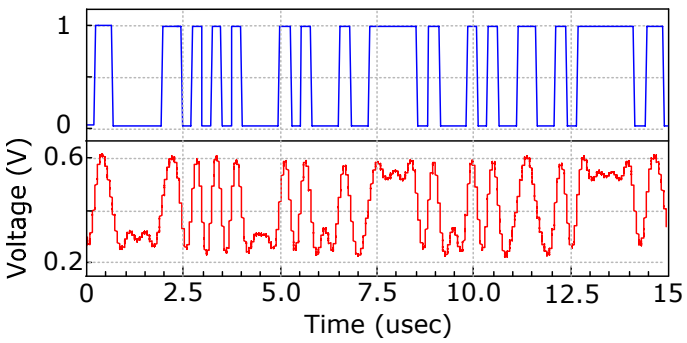

Figure 10.3.6: Measured 4Gb/s signal waveforms with BPSK modulation of the transceiver with and without the calibration procedure.

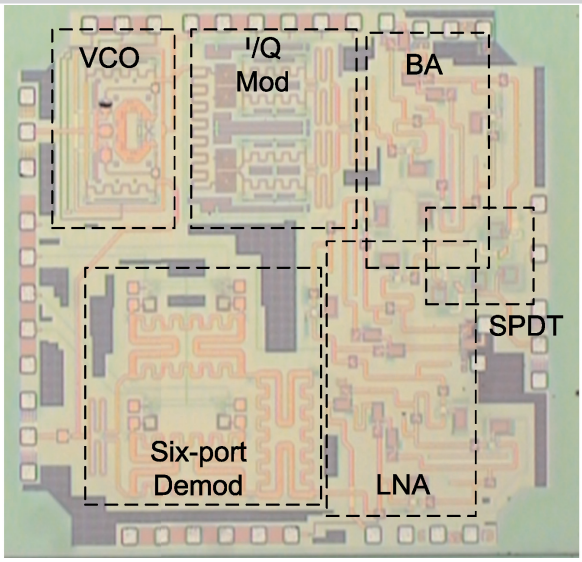

Figure 10.3.7: Chip micrograph of the 60GHz six-port transceiver (size: 1.65×1.5mm²).

